FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
57341-PCT (45107)	10/089570

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EPOO/09519	28 SEPTEMBER 2000	30 SEPTEMBER 1999 (30.09.1999)

TITLE OF INVENTION
ARRANGEMENT WITH IMAGE SENSORS

APPLICANT(S) FOR DO/EO/US
Infineon Technologies AG

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☒ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

PCT/RO/101
PCT/IB/304
PCT/OB/306
PCT/WO 01/24269

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/089570	PCT/EP00/09519	57341-PCT (45107)

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
	ENTER APPROPRIATE BASIC FEE AMOUNT =	**$890.00**
	Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$130.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	12 - 20 =	0	x $18.00	**$0.00**	
Independent claims	2 - 3 =	0	x $84.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
	TOTAL OF ABOVE CALCULATIONS =			**$1,020.00**	
☐	Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.			**$0.00**	
	SUBTOTAL =			**$1,020.00**	
	Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +			**$0.00**	
	TOTAL NATIONAL FEE =			**$1,020.00**	
☐	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			**$0.00**	
	TOTAL FEES ENCLOSED =			**$1,020.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$1,020.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **04-1105** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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33,860
REGISTRATION NUMBER

MARCH 29, 2002
DATE

Docket No. 57341

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Wolfgang KRUTSCHNEIDER; Heribert GEIB; Franz HOFMANN; and Till SCHLÖSSER

Express Mail Label No. EL 932681199US

For: ARRANGEMENT WITH IMAGE SENSORS

Assistant Commissioner For Patents
Washington, D.C. 20231
Sir:

PRELIMINARY AMENDMENT

Applicants herewith the above-identified application. Please amend the application as follows.

IN THE CLAIMS

Please cancel claims 1-7 without prejudice.

Please add the following new claims.

8. Arrangement with image sensors,

in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line or a reference line,

in which a gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,

in which the image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,

in which the image sensor has a photodiode, which is switched between a voltage connection and the gate electrode of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

9. Arrangement with image sensors,

in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line and a reference line,

in which one gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,

in which an image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,

in which an image sensor has a photodiode, which is switched between a voltage connection and the first source/drain area of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

10. Arrangement according to claim 8,

in which the photodiode consists of a n-doped area and a p-doped area adjacent to this, which is connected to the voltage connection.

11. Arrangement according to claim 10,

in which the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

12. Arrangement according to claim 8,

in which the memory transistor is designed as a vertical transistor,

in which the first source/drain area of the memory transistor is arranged over a second source/drain area of the memory transistor, which is connected to the reference line,

in which the reference line is buried in the substrate.

13. Arrangement according to claim 8,

in which the diode is designed as a tunnel diode and consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor.

14. Arrangement according to claim 13,

in which one substrate has a recess,

in which the recess extends into the reference line,

in which at least one lateral face of an upper area of the recess is provided with the insulating layer,

in which faces of a lower area of the recess lying below the upper part are equipped with a gate insulator,

in which the gate electrode of the memory transistors is arranged in the lower part,

in which the conductive structure of the diode arranged is in the upper part of the recess,

in which the first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area.

15. Arrangement according to claim 9,

in which the photodiode consists of a n-doped area and a p-doped area adjacent to this, which is connected to the voltage connection.

16. Arrangement according to claim 15,

in which the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

17. Arrangement according to claim 9,

in which the memory transistor is designed as a vertical transistor,

in which the first source/drain area of the memory transistor is arranged over a second source/drain area of the memory transistor, which is connected to the reference line,

in which the reference line is buried in the substrate.

18. Arrangement according to claim 9,

in which the diode is designed as a tunnel diode and consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor.

19. Arrangement according to claim 18,

in which one substrate has a recess,

in which the recess extends into the reference line,

in which at least one lateral face of an upper area of the recess is provided with the insulating layer,

in which faces of a lower area of the recess lying below the upper part are equipped with a gate insulator,

in which the gate electrode of the memory transistors is arranged in the lower part,

in which the conductive structure of the diode arranged is in the upper part of the recess,

in which the first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area.

REMARKS

Claims 1-7 have been cancelled without prejudice, and claims 8-19 have been added. No new matter has been added by virtue of the new claims.

Early consideration and allowance of the application are earnestly solicited.

Respectfully submitted,

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Description

Arrangement with image sensors

The invention relates to an arrangement with image sensors.

Image sensors are designed to produce electrical signals dependent on the intensity and colour of the projected light. To this end the image sensor includes a light-sensitive element. The light-sensitive element has a photoactive face. The light, which is projected onto the photoactive face, is converted by the light-sensitive element into an electrical signal. An arrangement with many image sensors is provided to record an image electrically, as is necessary for example in the case of a camera. The use of image sensors built on CMOS technology in contrast to image sensors built on CCD technology makes it possible to scan the individual image sensors independently from each other. To this end further elements as well as circuits are necessary in addition to the light sensitive elements. These further elements and circuits should only need as small a space as possible in order to achieve the best possible fill factor, that is to say the ratio between photoactive face and total face.

Such an arrangement with image sensors built on CMOS technology, which is suitable for a camera, is described for example in E. R. FOSSUM, "CMOS Image Sensors, Electronic Camera on a Chip," IEDM Dig. Techn. Pap., p.17, 1995. An image sensor includes as the light-sensitive element a photodiode and three MOS transistors. The circuitry of the transistors corresponds to the circuitry of the transistors in a 3 transistor DRAM cell arrangement. A first and a second transistor are connected in series and between a bit line and a reference line. A third transistor is connected between a gate electrode of the second transistor and the reference line. A gate electrode of the first transistor is connected to

a word line extending crosswise in relation to the bit line. A gate electrode of the third transistor is connected to a reset line. The photodiode is switched between a voltage connection and the gate electrode of the second transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

The invention is based on the problem of providing an arrangement with image sensors built on CMOS technology which is suitable for a camera and in regard to which an image sensor has a higher fill factor in comparison to the prior art.

The problem is solved by an arrangement with image sensors, in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line and a reference line. A gate electrode of the selection transistor is connected to a word line which extends crosswise in relation to the bit line. The image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor, in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction. The image sensor has a photodiode as the light-sensitive element, which is switched between a voltage connection and the gate electrode of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

A possible mode of operation of this arrangement is explained below:

The reference line is constantly held on an operating voltage V_{DD}. The voltage connection is constantly held on 0 Volt. The voltage connection can also be held on a negative voltage.

Reset of the image sensor:

The selection transistor is opened via the word line, the voltage V_{DD} is applied to the bit line. Voltage equalizing is achieved between the gate electrode of the memory transistor and V_{DD} via current conduction through the diode. After this (reset) operation V_{DD} lies on the gate electrode of the memory transistor.

"Measurement" of the image sensor:

With the selection transistor blocked, light falls onto the photodiode, as a result of which a voltage reduction occurs at the gate electrode of the memory transistor.

Read of the image sensor:

After a pre-set time (exposure time) the amount of projected light is determined by the opening of the selection transistor via the word line and the measurement of the signal arising on the bit line. To this end the bit line is previously discharged to earth. The signal on the bit line is dependent on the voltage at the gate electrode of the memory transistor at the start of the read operation. On the one hand the voltage difference between the gate electrode of the memory transistor and the first source/drain area of the memory transistor determines the strength of the current flowing through the memory transistor and therefore the bit line. On the other hand an equalizing current flows over a certain period between the gate electrode of the memory transistor and the first source/drain area of the memory transistor in the reverse direction of the diode until essentially the same voltage lies on the gate electrode of the memory transistor as on the first source/drain area of the memory transistor so that the memory transistor is blocked and no further current can flow onto the bit line. This period depends on the voltage at the gate electrode of the memory transistor at the start of the read operation. This voltage, which correlates with the

light incidence, thus determines the signal on the bit line in two respects.

After the read operation a reset is again started.

Since a pair, which consists of a word line and a bit line, is exactly associated with an image sensor, the individual image sensors of the arrangement can be scanned via the word lines and the bit lines. The signals on the bit lines are subsequently built up into an image. The arrangement is therefore suitable for a camera.

The problem is also solved by an arrangement with image sensors, in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line and a reference line. A gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line. The image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction. The image sensor has a photodiode, which is switched between a voltage connection and the first source/drain area of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

A possible mode of operation of such an arrangement is explained below:

The reference line is for example constantly held on an operating voltage V_{DD}. The voltage connection is for example constantly held on 0 Volt.

Reset of the image sensor:

The selection transistor is opened via the word line. The voltage V_{DD} lies on the bit line. An equalizing current flows via the diode between the gate electrode of the memory transistor and the first source/drain area of the memory transistor, until essentially V_{DD} lies on the gate electrode of the memory transistor.

"Measurement" of the image sensor:

With the selection transistor blocked light falls onto the photodiode, which leads to a reduction in the voltage at the first source/drain area of the memory transistor. An equalizing current flows via the diode in the reverse direction between the gate electrode of the memory transistor and the first source/drain area of the memory transistor, until essentially the same voltage lies on the gate electrode of the memory transistor as on the first source/drain area of the memory transistor. The light incidence on the photodiode consequently determines the voltage at the gate electrode of the memory transistor.

Read of the image sensor:

The selection transistor is opened via the word line. The signal arising on the bit line is measured. The read operation corresponds to the read operation of the image sensor already described above.

In contrast to the prior art the image sensor is connected with one line less, resulting in a better fill factor. Furthermore the diode can be produced more simply with less space requirement than a transistor, since the diode only has two inputs or outputs, while the transistor has three inputs or outputs (gate electrode and two source/drain areas). Also for this reason the image sensor has a higher fill factor than image sensors according to the prior art.

The diode does not need to meet high requirements. The ratio of current in the conducting direction to current in the reverse direction can be minimal. The diode can thus have a minimum asymmetry.

The readout time can be very short and can be chosen from between 10 ns and 20 ns for example.

The photodiode for example consists of a n-doped area and a p-doped area adjacent to this, which form a p-n transition. Either the n-doped area is arranged on the p-doped area or vice versa. One of the doped areas is wired to the voltage connection.

The colour sensitivity of the image sensor can be adjusted via the depth of the p-n transition of the photodiode. The thickness of the upper doped area, i.e. the depth of the p-n transition, is for example between 100 and 600 nm. The doping substance concentration of the upper doped area is for example between $5x10^{18}$ cm^{-3} and 10^{20} cm^{-3}. The doping substance concentration of the lower doped area is for example between 10^{16} cm^{-3} and 10^{18} cm^{-3}.

The photodiode can be connected via the substrate. For example the p-doped area is part of a well in the substrate. The voltage connection for example is adjacent to the substrate outside the arrangement of the image sensors.

To increase the fill factor it is advantageous if the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

To increase the fill factor it is advantageous if the memory transistor is designed as a vertical transistor. The memory

transistor owing to its vertical arrangement has lesser space requirement than if it were designed as a planar transistor.

The first source/drain area of the memory transistor is preferably arranged over a second source/drain area of the memory transistor, which is connected to the reference line. As a result the fill factor is increased, since the reference line is buried in the substrate and therefore the photodiode cannot create a shadow. The photodiode consequently can be arranged over the reference line in such a way that the reference line does not reduce the fill factor.

The diode can be designed as a tunnel diode. A particularly high fill factor can be achieved if the diode is integrated with the memory transistor, since then it does not require any space additional to the memory transistor. The diode in this case consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor. The conductive structure, as the gate electrode of the memory transistor, consists preferably of doped polysilicon. So that the reverse direction of the diode points in the right direction, the doping substance concentration of the conductive structure is less than that of the gate electrode and less than that of the first source/drain area of the memory transistor.

It is within the scope of the invention if a substrate has a recess, which extends into the reference line. At least one lateral face of an upper area of the recess is provided with the insulating layer. The insulating layer consequently lies essentially vertically to a surface of the substrate, from which the recess originates. Faces of a lower part of the recess lying below the upper part are provided with a gate insulator. The gate electrode of the memory transistor is arranged in the lower part. The conductive structure of the

diode is arranged in the upper area of the recess. Thus the conductive structure is arranged on the gate electrode. The first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area. Part of the reference line acts as second source/drain area of the memory transistor.

The fill factor can be further increased if the selection transistor is designed as a vertical transistor. Alternatively the selection transistor is designed as a planar transistor.

The image sensors for example are arranged in rows and columns. The bit lines and word lines extend along the rows and the columns.

Embodiments of the invention are explained in more detail below by way of the figures.

Figure 1 shows the circuit of a first image sensor.

Figure 2a shows a top view onto a first substrate with the first image sensor, in which a reference line, a word line, a gate electrode and a first source/drain area of a memory transistor, a conductive structure, a n-doped area of a photodiode, a first source/drain area and a second source/drain area of the selection transistor and a bit line are shown.

Figure 2b shows a section through the top view from Figure 2a, in which a gate insulator, the gate electrode of the memory transistor, the conductive structure, the word line, the reference line, the bit line, an intermediate oxide, contacts, the first source/drain area of the memory transistor, the first source/drain area of a selection transistor, the

second source/drain area of the selection transistor, an insulating layer and a second source/drain area of the memory transistor are shown.

Figure 3 shows the circuit of a second image sensor.

Figure 4a shows the top view onto a second substrate with a second image sensor, in which a reference line, a word line, a bit line, a gate electrode, a first source/drain area and a second source/drain area of a memory transistor, a first source/drain area and a second source/drain area of a selection transistor, a conductive structure and a n-doped area of a photodiode are shown.

Figure 4b shows a cross-section through the second substrate, in which the bit line, an intermediate oxide, a contact, the word line, the reference line, the gate electrode, the first source/drain area and the second source/drain area of the memory transistor, the conductive structure, the n-doped area of the photodiode, an insulating layer, the first source-/drain area and the second source/drain area of the selection transistor and a gate insulator are shown.

Figure 5a shows a top view onto a third substrate with a third image sensor, in which a word line, a bit line, a n-doped area of a photodiode, a first and a second source/drain area of a selection transistor, a first source/drain area of a memory transistor and a line are shown.

Figure 5b shows a first cross-section through the third substrate, in which the line, contacts, the word line, the bit line, an intermediate oxide, a recess,

a conductive structure, an insulating layer, a gate electrode and a first source drain area of a memory transistor, a first source/drain area and a second source/drain area of the selection transistor, an intermediate oxide, a reference line and a gate insulator are shown.

Figure 5c shows a second cross-section through the third substrate vertical to the first cross-section, in which the line, contacts, the bit line, the n-doped area of the photodiode, an insulation, the recess, a conductive structure, an insulating layer, the gate electrode of the memory transistor, the gate insulator, the reference line and the intermediate oxide are shown.

Figure 6a shows a top view onto a fourth substrate with a fourth image sensor, in which a word line, a bit line, a n-doped area of a photodiode, a first source/drain area and a second source/drain area of a selection transistor, a first source/drain area of a memory transistor and a conductive structure are shown.

Figure 6b shows a cross-section through the fourth substrate, in which the n-doped area of the photodiode, the conductive structure, an insulation, a gate electrode of the memory transistor, a reference line, the bit line, an intermediate oxide and a gate insulator are shown.

Figure 7a shows a top view onto a fifth substrate with a fifth image sensor, in which a word line, a bit line, a first and a second source/drain area of a selection transistor, a first source/drain area of a memory

transistor, a n-doped area of a photodiode and a conductive structure are shown.

Figure 7b shows the cross-section through the fifth substrate, in which a recess, the conductive structure, a gate electrode and the first source/drain area of the memory transistor, a gate insulator, an insulating layer, the n-doped area of the photodiode, the word line, the first and the second source/drain area of the selection transistor, the bit line, an intermediate oxide, a contact and a reference line are shown.

Figure 8 shows a top view onto a sixth substrate with a sixth image sensor, in which a n-doped area of a photodiode, a first and a second source/drain area of a selection transistor, a first source/drain area of a memory transistor, a conductive structure, a word line and a bit line are shown.

The figures are not drawn to scale.

In a first embodiment a first image sensor of an arrangement with image sensors includes a memory transistor TV1, a selection transistor TR1, a diode ID1 and a photodiode FD1, which are connected to each other according to claim 1 (see Figure 1).

The memory transistor TV1 and the selection transistor TR1 are designed as planar MOS-transistors in the vicinity of a surface of a first substrate 1. The first substrate 1 has a doping substance concentration of approx. 10^{17} cm^{-3} and is p-doped in the vicinity of the transistor. This area is also described as well. The first source/drain area of the memory transistor TV1 and a first source/drain area of the selection

transistor TR1 form a cohesive n-doped area S/D1 in the first substrate 1.

The doped area S/D1, a second n-doped source/drain area SI of the memory transistor TV1 and a second n-doped source/drain area A1 of the selection transistor TR1 are arranged in a row next to each other, at a distance from each other and comprise a doping substance concentration of approx. $10^{20}cm^{-3}$. The doped area S/D1, the second n-doped source/drain area S1 of the memory transistor TV1 and the second n-doped source/drain area A1 of the selection transistor TR1 comprise a square horizontal cross-section, that is to say parallel to the surface of the first substrate 1 with a side length of approx. 250 nm.

Between the second source/drain area Al of the selection transistor TR1 and the doped area S/D1 a gate electrode of the selection transistor TRl is arranged on the first substrate 1, which is part of a word line W1 (see Figures 2a and 2b). The word line W1 is approx. 250 nm wide.

Between the doped area S/D1 and the second source/drain area S1 of the memory transistor TV1 a gate electrode G1 of the memory transistor TV1 is arranged on the first substrate 1. The gate electrode G1 of the memory transistor TV1 consists of n-doped polysilicon and has a doping substance concentration of approx. 10^{20} cm^{-3}. The gate electrode G1 of the memory transistor TV1 has a square horizontal parallel cross-section with a side length of approx. 250 nm.

A gate insulator GD1 separates the word line W1 and the gate electrode G1 of the memory transistor TV1 from the first substrate 1.

An insulating layer I1 is arranged on the doped area S/D1, which is adjacent to the gate electrode G1 of the memory

transistor TV1 (see Figure 2b). A conductive structure L1 is arranged on the insulating layer I1, which overlaps the gate electrode G1 of the memory transistor TV1. The conductive structure L1 can for example be produced by precipitating and structuring a layer deposited in a conform way from n-doped polysilicon. The conductive structure L1 is n-doped and has a doping substance concentration of approx. 10^{19} cm^{-3}. A dimension parallel to the bit line B1 of the conductive structure L1 is approx 250 nm. A dimension parallel to the word line W1 of the conductive structure L1 is approx. 250 nm.

Adjacent to the surface of the first substrate 1 an approx. 200 nm thick n-doped area N1 of the photodiode FD1 is arranged at a distance of approx. 250 nm from the doped area S/DI. A dimension vertical to the word line W1, which is parallel to the surface of the substrate 1, of the n-doped area N1 of the photodiode FD1 is approx. 800 nm. A dimension parallel to the word line W1, which is parallel to the surface of the substrate 1, of the n-doped area N1 of the photodiode FD1 is approx. 600 nm. Under the n-doped area N1 a p-doped area (not shown) of the photodiode FD1 acts as part of the first substrate 1.

The conductive structure L1 extends from the doped area S/D1 up to the n-doped area N1 of the photodiode FD1. Between the doped area S/D1 and the n-doped area N1 of the photodiode FD1 the conductive structure L1 is separated by an insulation (not shown) from the first substrate 1. The conductive structure L1 is adjacent to the n-doped area N1 of the photodiode FD1 from above.

An approx. 800 nm thick first part of an intermediate oxide Z1 consisting of SiO_2 is arranged on the first substrate 1. The reference line R1 is arranged on the first part of the intermediate oxide Z1, which is connected via a contact KR1 to

the second source/drain area S1 of the memory transistor TV1. The reference line R1 extends parallel to the word line W1.

An approx. 800 nm thick second part of the intermediate oxide Z1 is arranged on the first part of the intermediate oxide Z1. The bit line BI is arranged on the second part of the intermediate oxide Z1, which extends vertically to the word line W1 and is connected via a contact KB1 to the second source/drain area A1 of the selection transistor TR1.

The word line W1 and the reference line R1 shade parts of the n-doped area N1 of the photodiode FD1 in such a way that the photoactive face of the photodiode FD1 is smaller than the n-doped area N1 of the photodiode FD1.

The diode ZD1 is formed by the doped area S/D1, the insulating layer I1 and the conductive structure L1.

An operating voltage V_{DD}, which is approx. 3.3 V, constantly lies on the reference line R1. 0V lies on the well in the first substrate 1 and consequently on the p-doped area of the photodiode FD1. The well is wired via a voltage connection (not shown).

In a second embodiment a second image sensor of an arrangement with image sensors includes a selection transistor TR2, a memory transistor TV2, a diode 1D2 and a photodiode FD2, which are connected according to claim 2 (see Figure 3).

The first source/drain area of the memory transistor TV2, a first source/drain area of the selection transistor TR2 and a n-doped area of the photodiode FD2 are arranged as cohesive doped area S/D2 in the second substrate 2 (see Figures 4a and 4b). The doped area S/D2 is adjacent to a surface of the second substrate 2.

The memory transistor TV2 and the selection transistor TR2 are designed as in the first embodiment. The doped area S/D2, a second source/drain-area S2 of the memory transistor TV2 and a second source/drain area A2 of the selection transistor TR2 are arranged in a row next to each other and at a distance from each other (see Figure 4b). Between the doped area S/D2 and the second source/drain area A2 of the selection transistor the gate electrode of the selection transistor is arranged on the second substrate 2, which is part of a word line W2 and is separated by a gate insulator GD2 from the second substrate 2 (see Figures 4a and 4b).

The second source/drain area S2 of the memory transistor TV2 is part of the reference line R2, which extends as strip-shaped doped area parallel to the word line W2.

An insulating layer I2 and the gate electrode G2 of the memory transistor TV2 are arranged as in the first embodiment (see Figures 4a and 4b). The doped area S/D2 is arranged in a horseshoe-shape around half the gate electrode G2 of the memory transistor TV2 (see Figure 4a). In order to prevent short-circuits the doped area S/D2 does not extend up to the reference line R2.

A conductive structure L2 consisting of n-doped polysilicon is arranged on the insulating layer I2 and on the gate electrode G2 of the memory transistor (see Figure 4b). In contrast to the first embodiment, the conductive structure L2 is not adjacent in the vicinity of the photodiode FD2 to the second substrate 2. The conductive structure L2 is square from the top view with a side length of approx. 250 nm.

An approx. 800 nm thick intermediate oxide Z2 consisting of SiO2 is arranged on the second substrate 2. The bit line B2 is arranged on the intermediate oxide Z2, which extends vertically to the word line W2 and is connected via a contact

KB2 to the second source/drain area A2 of the selection transistor TR2.

In a third embodiment a third substrate is provided with a third image sensor of an arrangement with image sensors, which has a selection transistor, a memory transistor, a diode and a photodiode, which are connected as in the first embodiment (see Figure 1).

In contrast to the first embodiment the memory transistor is designed as a vertical MOS transistor. To this end an approx. 500 nm deep recess V3 is provided in the third substrate 3. Approx. 400 nm below a surface of the third substrate 3, from which the recess V3 originates, the reference line R3 is arranged in the form of a n-doped layer of the third substrate 3. The doping substance concentration of the reference line R3 is approx. 10^{19} cm^{-3} (see Figures 5b and 5c). The recess V3 thus extends into the reference line R3. The reference line R3 serves as common reference line for all image sensors of the arrangement.

An approx. 2 nm thick insulating layer I3 consisting of SiO_2 is arranged on a lateral face of an upper area of the recess V3 (see Figure 5b). In contrast to the insulating layers I1, I2 in the first two embodiments, the insulating layer I3 in this embodiment lies vertically to the surface of the third substrate 3. The insulating layer I3 extends approx. 100 nm into the third substrate 3.

Other faces of the recess V3 are provided with an approx. 6 nm thick gate insulator GD3 consisting of SiO_2 (see Figures 5b and 5c).

The gate electrode G3 of the memory transistor is arranged in a lower part of the recess V3 lying under the upper part. The

gate electrode G3 of the memory transistor fills the recess V3 up to a height of approx. 100 nm.

A conductive structure L3 consisting of n-doped polysilicon is arranged over the gate electrode G3 of the memory transistor. The conductive structure L3 has a doping substance concentration of approx. 10^{19} cm^{-3}. The gate electrode G3 of the memory transistor and the conductive structure L3 together fill up the recess V3.

The first source/drain area of the memory transistor and a first source/drain area of the selection transistor form a cohesive n-doped area S/D3 in the third substrate 3, which is adjacent to the lateral face of the upper area of the recess V3, that is to say the insulating layer I3 (see Figure 5b). The doped area S/D3 has a doping substance concentration of approx. 10^{20} cm^{-3}.

Part of the reference line R3, which is adjacent to the recess V3, acts as second source/drain area of the memory transistor.

An approx. 300 nm thick n-doped area N3 of the photodiode is provided in the substrate S3 adjacent to the surface of the third substrate 3, which is at a distance from the doped area S/D3. The n-doped area N3 has a doping substance concentration of approx. 10^{20} cm^{-3} and is rectangular with side lengths of 800 nm and 600 nm (see Figures 5a and 5c). The n-doped area N3 is embedded in a p-doped area of the photodiode, which is part of a p-doped well in the third substrate 3 (see Figure 5c).

The diode is formed by the doped area S/D3, the insulating layer 13 and the conductive structure L3.

The second source/drain area A3 of the selection transistor is designed as the selection transistor in embodiment 2 or embodiment 1. The same applies to the word line W3, which is

separated by the gate insulator GD3 from the third substrate 3.

Between the n-doped area N3 and the recess V3 an insulation IS3 is provided in the third substrate.

An approx. 800 nm thick first part of an intermediate oxide Z3 consisting of SiO_2 is arranged on the third substrate 3 (see Figures 5b and 5c). Contacts K3 are arranged in the first part of the intermediate oxide Z3, which contact the conductive structure Z3 and the n-doped area N3 of the photodiode (see Figure 5b).

The contacts K3 are connected with each other via a line Q3 arranged on the first part of the intermediate oxide Z3 (see Figures 5a and 5c).

An approx. 800 nm thick second part of the intermediate oxide Z3 is arranged on the first part of the intermediate oxide Z3. The bit line B3 is arranged on the second part of the intermediate oxide Z3 which extends vertically to the word line W3 and is connected via a contact B3 to the second source/drain area A3 of the selection transistor.

In a fourth embodiment a fourth substrate 4 is provided with a fourth image sensor of an arrangement with image sensors, which has a selection transistor, a memory transistor, a diode and a photodiode, which are connected as in the third embodiment (see Figure 1).

The fourth image sensor is essentially designed as the third image sensor with the difference that no line is provided with associated contacts, which connects the conductive structure L4 to the n-doped area N4 of the photodiode. Instead the conductive structure L2 extends laterally up to the n-doped area N4 of the photodiode. The conductive structure L4 is

arranged on the insulation IS4, the consequence of which is that the conductive structure L4 is only adjacent in the section of the n-doped area N4 of the photodiode to the fourth substrate 4 (see Figures 6a and 6b).

An approx. 800 nm thick intermediate oxide Z4 consisting of SiO_2 is provided, on which the bit line B4 is arranged and is connected via a contact (not shown) to the second source/drain area of the selection transistor.

As in the third embodiment a gate insulator GD4, a gate electrode G4 of the memory transistor, a common doped area S/D4, a second source/drain area A4 of the selection transistor, a reference line R4, a word line W4, a bit line B4 and an insulation IS4 are provided.

In a fifth embodiment a fifth substrate 5 is provided with a fifth image sensor of an arrangement with image sensors, which has a selection transistor, a memory transistor, a photodiode and a diode, which are connected as in the second embodiment (see Figure 3).

The memory transistor, the selection transistor, an insulating layer I5, the word line W5, the reference line R5 and the bit line B5 are designed as in the fourth embodiment (see Figures 7a and 7b). Thus a second source/drain area A5 of the selection transistor, a gate insulator GD5, a contact KB5 to the bit line B5, an intermediate oxide 25 and a gate electrode G5 of the memory transistor are provided in a recess V5 as in the fourth embodiment.

In contrast to the fourth embodiment the n-doped area of the photodiode, the first source/drain area of the memory transistor and a first source/drain area of the selection transistor form a cohesive n-doped area S/D5. The doped area S/D5 has a rectangular cross-section with side lengths of

approx. 700 nm and 800 nm. The lateral distance between the recess V5 and the word line W5 is 700 nm. The conductive structure L5 of the diode is arranged completely inside the recess V5 and is not adjacent to the fifth substrate 5 (see Figures 7a and 7b).

In a sixth embodiment a sixth substrate 6 is provided with a sixth image sensor of an arrangement with image sensors, which is designed corresponding to the fifth image sensor, with the difference that a lateral distance between the recess and the word line W6 is only 250 nm and the doped area S/D6 extends beyond an area between the recess and the word line W6 (see Figure 8).

As in the fifth embodiment a first source/drain area of the selection transistor, a first source/drain area of the memory transistor and a n-doped area of the photodiode form a common doped area S/D6. As in the fifth embodiment the gate electrode of the memory transistor and the conductive structure L6 are arranged in a recess. As in the fifth embodiment a second source/drain area of the selection transistor and the bit line B6 are provided.

Many variations of the embodiments, which also fall within the scope of the invention, are conceivable. Thus dimensions of the described layers, structures, lines and areas can be adapted to the particular requirements. The same applies for the choice of the materials and for the doping substance concentrations.

Art 34 amendment

Patent claims

1. Arrangement with image sensors,
- in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line or a reference line,
- in which a gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,
- in which the image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,
- in which the image sensor has a photodiode, which is switched between a voltage connection and the gate electrode of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

2. Arrangement with image sensors,
- in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line and a reference line,
- in which one gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,
- in which an image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,
- in which an image sensor has a photodiode, which is switched between a voltage connection and the first source/drain area

of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

3. Arrangement according to claim 1 or 2,
- in which the photodiode consists of a n-doped area and a p-doped area adjacent to this, which is connected to the voltage connection.

4. Arrangement according to claim 3,
- in which the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

5. Arrangement according to one of claims 1 to 4,
- in which the memory transistor is designed as a vertical transistor,
- in which the first source/drain area of the memory transistor is arranged over a second source/drain area of the memory transistor, which is connected to the reference line,
- in which the reference line is buried in the substrate.

6. Arrangement according to one of claims 1 to 5,
- in which the diode is designed as a tunnel diode and consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor.

7. Arrangement according to claim 6,
- in which one substrate has a recess,
- in which the recess extends into the reference line,
- in which at least one lateral face of an upper area of the recess is provided with the insulating layer,
- in which faces of a lower area of the recess lying below the upper part are equipped with a gate insulator,

- in which the gate electrode of the memory transistors is arranged in the lower part,
- in which the conductive structure of the diode arranged is in the upper part of the recess,
- in which the first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area.

Abstract

Arrangement with image sensors

A memory transistor and a selection transistor of an image sensor are connected in series and between a bit line (B5) and a reference line (R5). A gate electrode of the selection transistor is connected to a word line (W5), which extends crosswise in relation to the bit line (B5). A diode of the image sensor is switched between a gate electrode (G5) of the memory transistor and a first source/drain area (S/D5) of the memory transistor, which is connected to the selection transistor in such a way is polarised towards the first source/drain area (S/D5) of the memory transistor and in the reverse direction. A photodiode of the image sensor is switched between a voltage connection and either the gate electrode (G5) of the memory transistor or the first source/drain area (S/D5) of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

Figure 7b

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Declaration and Power of Attorney for Patent Application
English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"ARRANGEMENT WITH IMAGE SENSORS"

the specification of which

(check one)

[ ] is attached hereto.
[X] was filed on 28 September 2000 as United States Application No. or PCT Application No. PCT/EP00/09519
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
DE 199 46 983.0 (Number)	Germany (Country)	30 September 1999 (Day/Month/Year Filed)	[ ]
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	[ ]
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I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

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(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
PCT/EP00/09519	28 September 2000	Pending

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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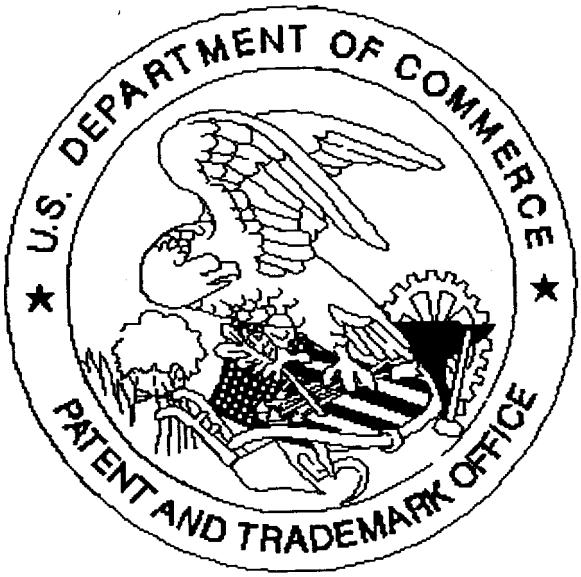

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